What is claimed is:

1. A semiconductor integrated circuit having a contact array in which a plurality of contacts is formed so as to be aligned in a vertical direction and a horizontal direction,

wherein a contact formation spacing in one of the vertical and the horizontal directions in the contact array is larger than a contact formation spacing determined by a manufacturing process.

2. A semiconductor integrated circuit having a contact array in which a plurality of contacts is formed so as to be aligned in a vertical direction and a horizontal direction,

wherein a contact formation spacing in both of the vertical and the horizontal directions in the contact array is larger than a contact formation spacing determined by a manufacturing process.

3. A semiconductor integrated circuit having a contact array in which a plurality of contacts is formed so as to be aligned in a vertical direction and a horizontal direction,

wherein the contact array is formed by placing a first contact array unit and a second contact array unit one on another, the first and the second contact array units have a structure in which a plurality of contacts is formed so as to be aligned in the vertical and the horizontal directions, a contact

formation spacing in at least one of the vertical and the horizontal directions in each of the first and the second contact array units is larger than a contact formation spacing determined by a manufacturing process, and the first and the second contact array units are placed one on another so as to be shifted from each other so that contact formation positions of the first contact array unit are situated midway between contact formation positions of the second contact array unit both in the vertical and the horizontal directions.

4. A semiconductor integrated circuit having a contact array in which a plurality of contacts is formed so as to be aligned in a vertical direction and a horizontal direction,

wherein an entire area of a chip is swept while overlap of regions of a unit area determined by a manufacturing process is allowed, a number or an area of the contacts formed so as to be aligned in the vertical and the horizontal directions which contacts are present in the regions of the unit area is obtained, and a contact formation spacing is increased so that the number or the area of the contacts included in the regions of the unit area is not more than a predetermined value.

5. A semiconductor integrated circuit according to claim 1, wherein a rate of reduction of the number of contacts when the contact formation spacing is increased is varied according

to a size of the contact array.

6. A semiconductor integrated circuit according to claim 2, wherein a rate of reduction of the number of contacts when the contact formation spacing is increased is varied according to a size of the contact array.

7. A semiconductor integrated circuit according to claim 3, wherein a rate of reduction of the number of contacts when the contact formation spacing is increased is varied according to a size of the contact array.

8. A semiconductor integrated circuit according to claim 4, wherein a rate of reduction of the number of contacts when the contact formation spacing is increased is varied according to a size of the contact array.

9. A semiconductor integrated circuit having a contact array in which a plurality of contacts is formed so as to be aligned in a vertical direction and a horizontal direction,

wherein the contact array is divided into at least two contact array regions, and in at least one of the contact array regions, the contacts are formed at spacings not less than contact formation spacings determined by a manufacturing process and in a remaining contact array region, the contacts

are formed at contact formation spacings larger than the contact formation spacing in the at least one of the contact array regions.

10. A semiconductor integrated circuit having a contact array in which a plurality of contacts is formed so as to be aligned in a vertical direction and a horizontal direction,

wherein the contact array is divided into at least three contact array regions, a number or an area of the contacts present in a region of a unit area is obtained, and the contacts are formed at spacings not less than contact formation spacings determined by a manufacturing process in each of at least two of the contact array regions arranged at predetermined region spacings so that the number or the area of contacts included in the region of the unit area is not more than a predetermined value.

11. A semiconductor integrated circuit according to claim 1, wherein at least three layers of contact arrays are longitudinally laminated, and in a contact array of an intermediate layer, as a result of increasing a contact formation spacing, contacts remaining in the contact array of the intermediate layer are re-arranged at spacings not less than contact spacings determined by a process, whereby a region of the contact array of the intermediate layer is smaller than

regions of contact arrays of an uppermost layer and a lowermost layer.

12. A semiconductor integrated circuit according to claim 2, wherein at least three layers of contact arrays are longitudinally laminated, and in a contact array of an intermediate layer, as a result of increasing a contact formation spacing, contacts remaining in the contact array of the intermediate layer are re-arranged at spacings not less than contact spacings determined by a process, whereby a region of the contact array of the intermediate layer is smaller than regions of contact arrays of an uppermost layer and a lowermost layer.

13. A semiconductor integrated circuit according to claim 3, wherein at least three layers of contact arrays are longitudinally laminated, and in a contact array of an intermediate layer, as a result of increasing a contact formation spacing, contacts remaining in the contact array of the intermediate layer are re-arranged at spacings not less than contact spacings determined by a process, whereby a region of the contact array of the intermediate layer is smaller than regions of contact arrays of an uppermost layer and a lowermost layer.

14. A semiconductor integrated circuit according to claim 4, wherein at least three layers of contact arrays are longitudinally laminated, and in a contact array of an intermediate layer, as a result of increasing a contact formation spacing, contacts remaining in the contact array of the intermediate layer are re-arranged at spacings not less than contact spacings determined by a process, whereby a region of the contact array of the intermediate layer is smaller than regions of contact arrays of an uppermost layer and a lowermost layer.

15. A method of manufacturing a semiconductor integrated circuit having a contact array in which a plurality of contacts is formed so as to be aligned in a vertical direction and a horizontal direction,

wherein a contact formation spacing in one of the vertical and the horizontal directions in the contact array is larger than a contact formation spacing determined by a manufacturing process.

16. A method of manufacturing a semiconductor integrated circuit having a contact array in which a plurality of contacts is formed so as to be aligned in a vertical direction and a horizontal direction,

wherein a contact formation spacing in both of the

vertical and the horizontal directions in the contact array is larger than a contact formation spacing determined by a manufacturing process.

17. A method of manufacturing a semiconductor integrated circuit having a contact array in which a plurality of contacts is formed so as to be aligned in a vertical direction and a horizontal direction,

wherein when the contact array is formed by placing one on another a first contact array unit and a second contact array unit in which a plurality of contacts is formed so as to be aligned in the vertical and the horizontal directions, a contact formation spacing in at least one of the vertical and the horizontal directions in each of the first and the second contact array units is larger than a contact formation spacing determined by a manufacturing process, and the first and the second contact array units are placed one on another so as to be shifted from each other so that contact formation positions of the first contact array unit are situated midway between contact formation positions of the second contact array unit both in the vertical and the horizontal directions.

18. A method of manufacturing a semiconductor integrated circuit having a contact array in which a plurality of contacts is formed so as to be aligned in a vertical direction and a

horizontal direction,

wherein an entire area of a chip is swept while overlap of regions of a unit area determined by a manufacturing process is allowed, a number or an area of the contacts formed so as to be aligned in the vertical and the horizontal directions which contacts are present in the regions of the unit area is obtained, and a contact formation spacing is increased so that the number or the area of the contacts included in the regions of the unit area is not more than a predetermined value.

19. A method of manufacturing a semiconductor integrated circuit according to claim 15, wherein a rate of reduction of the contacts when the contact formation spacing is increased is varied according to a size of the contact array.

20. A method of manufacturing a semiconductor integrated circuit according to claim 16, wherein a rate of reduction of the contacts when the contact formation spacing is increased is varied according to a size of the contact array.

21. A method of manufacturing a semiconductor integrated circuit according to claim 17, wherein a rate of reduction of the contacts when the contact formation spacing is increased is varied according to a size of the contact array.

22. A method of manufacturing a semiconductor integrated circuit according to claim 18, wherein a rate of reduction of the contacts when the contact formation spacing is increased is varied according to a size of the contact array.

23. A method of manufacturing a semiconductor integrated circuit having a contact array in which a plurality of contacts is formed so as to be aligned in a vertical direction and a horizontal direction,

wherein the contact array is divided into at least two contact array regions, and in at least one of the contact array regions, the contacts are formed at spacings not less than contact formation spacings determined by a manufacturing process and in a remaining contact array region, the contacts are formed at contact formation spacings larger than the contact formation spacing in the at least one of the contact array regions s.

24. A method of manufacturing a semiconductor integrated circuit having a contact array in which a plurality of contacts is formed so as to be aligned in a vertical direction and a horizontal direction,

wherein the contact array is divided into at least three contact array regions, a number or an area of the contacts present in a region of a unit area is obtained, and the contacts

are formed at spacings not less than contact formation spacings determined by a manufacturing process in each of at least two of the contact array regions arranged at predetermined region spacings so that the number or the area of contacts included in the region of the unit area is not more than a predetermined value.

25. A method of manufacturing a semiconductor integrated circuit according to claim 15, wherein at least three layers of contact arrays are longitudinally laminated, and in a contact array of an intermediate layer, as a result of increasing a contact formation spacing, contacts remaining in the contact array of the intermediate layer are re-arranged at spacings not less than contact spacings determined by a process, whereby a region of the contact array of the intermediate layer is smaller than regions of contact arrays of an uppermost layer and a lowermost layer.

26. A method of manufacturing a semiconductor integrated circuit according to claim 16, wherein at least three layers of contact arrays are longitudinally laminated, and in a contact array of an intermediate layer, as a result of increasing a contact formation spacing, contacts remaining in the contact array of the intermediate layer are re-arranged at spacings not less than contact spacings determined by a process, whereby a

region of the contact array of the intermediate layer is smaller than regions of contact arrays of an uppermost layer and a lowermost layer.

27. A method of manufacturing a semiconductor integrated circuit according to claim 17, wherein at least three layers of contact arrays are longitudinally laminated, and in a contact array of an intermediate layer, as a result of increasing a contact formation spacing, contacts remaining in the contact array of the intermediate layer are re-arranged at spacings not less than contact spacings determined by a process, whereby a region of the contact array of the intermediate layer is smaller than regions of contact arrays of an uppermost layer and a lowermost layer.

28. A method of manufacturing a semiconductor integrated circuit according to claim 18, wherein at least three layers of contact arrays are longitudinally laminated, and in a contact array of an intermediate layer, as a result of increasing a contact formation spacing, contacts remaining in the contact array of the intermediate layer are re-arranged at spacings not less than contact spacings determined by a process, whereby a region of the contact array of the intermediate layer is smaller than regions of contact arrays of an uppermost layer and a lowermost layer.

29. A semiconductor integrated circuit having a contact array in which a plurality of contacts is formed so as to be aligned in a vertical direction and a horizontal direction,

wherein the contact array comprises contacts in odd-numbered rows and contacts in even-numbered rows disposed in positions shifted by substantially half a pitch from the contacts in the odd-numbered rows in a direction of the rows, and at least one of a contact spacing of the contacts in the odd-numbered rows and a contact spacing of the contacts in the even-numbered rows, and a spacing between the rows of the contacts in the odd-numbered rows and a spacing between the rows of the contacts in the even-numbered rows are larger than a contact formation spacing determined by a manufacturing process.

30. A semiconductor integrated circuit according to claim 29, wherein a rate of reduction of the number of contacts when the contact formation spacing is increased is varied according to a size of the contact array.